

WHAT IS CLAIMED IS:

1 1. A trenched DMOS device formed atop an N⁺ silicon substrate with
2 an N epitaxial layer thereon including a device region and a bus region neighboring the
3 device region, the device region comprising:

4 a P substrate, formed in the epitaxial layer and extending to a top
5 surface thereof, a plurality of DMOS trenches extending downward through the P
6 substrate from a top surface thereof;

7 a gate oxide layer formed in the DMOS trenches and extending to
8 cover the top surface of the P substrate;

9 a plurality of polysilicon gates formed in the DMOS trenches;

10 a plurality of N⁺ source regions formed in the P substrate adjacent
11 the DMOS trenches;

12 a plurality of P⁺ diffused regions formed in the P substrate and each
13 being interposed between two of the N⁺ source regions;

14 a first isolation layer formed over the P substrate to cover the
15 polysilicon gate electrodes; and

16 a source metal contact layer formed on the first isolation layer and
17 connecting to the N⁺ source regions and the P⁺ diffused regions;
18 and the bus region comprising:

19 a P substrate, formed in the epitaxial layer and extending to a top
20 surface of the epitaxial layer, a field oxide layer being formed on the P substrate and a bus
21 trench extending down from a top surface of the field oxide layer to a lower portion of the
22 P substrate;

23 a gate oxide layer formed in the bus trench and extending to cover a
24 top surface of the P substrate;

25 a polysilicon bus formed in the bus trench and having a top surface
26 disposed at a lower level than the top surface of the field oxide layer;

27 a second isolation layer covering the field oxide layer and having an
28 opening to expose the polysilicon bus; and

29 a metal line formed atop the polysilicon bus.

1 2. The trench DMOS device of claim 1, wherein the P substrate of
2 the device region and the P substrate of the bus region are formed by ion implantation
3 simultaneously.

1 3. The trench DMOS device of claim 1, wherein the gate oxide layer
2 of the device region and the gate oxide layer of the bus region are formed simultaneously.

1 4. The trench DMOS device of claim 1, wherein the polysilicon gate
2 and the polysilicon bus are formed by depositing a polysilicon layer in the DMOS trenches
3 and the bus trench and using the gate oxide layers as etch stop layers to etch the
4 polysilicon layer.

1 5. The trench DMOS device of claim 1, wherein the plurality of N+
2 source regions are formed in the P substrate on opposite sides of each of the DMOS
3 trenches.

1 6. A semiconductor device set which comprises at least two types of
2 devices, each of the two types of devices having a trench feature;
3 wherein the first device comprises a gate oxide formed in the trench
4 feature, a polysilicon layer formed on the gate oxide in the trench features, a first isolation
5 layer formed on the polysilicon layer and having an opening, and a metal layer formed on
6 the first isolation layer and filling the opening of the first isolation layer; and
7 wherein the second device comprises a dielectric layer formed
8 adjacent an opening at a top of the trench feature on opposite sides of the trench feature, a
9 gate oxide formed in the trench feature and over the dielectric layer, a polysilicon layer
10 formed on the gate oxide in the trench feature including a space near the top of the trench
11 feature with the dielectric layer disposed on opposite sides thereof, a second isolation layer
12 formed on the dielectric layer, and a metal layer formed on the polysilicon layer.

1 7. The semiconductor device set of claim 6, wherein the at least two
2 types of devices are formed on a silicon substrate.

1 8. The semiconductor device set of claim 7, wherein the silicon
2 substrate has an epitaxial layer formed thereon.

1 9. The semiconductor device set of claim 8, wherein the epitaxial layer
2 has a P substrate thereon.

1 10. The semiconductor device set of claim 9, wherein each trench
2 feature extends through the P substrate to an area below a top surface of the epitaxial
3 layer.

1 11. The semiconductor device of claim 9, wherein a plurality of N
2 source regions and a plurality of P regions are formed in the P substrate.

1 12. The semiconductor device of claim 11, wherein at least two of the N
2 source regions formed in the P substrate are disposed adjacent to and on opposites sides of
3 one of the first devices, and wherein at least one of the P regions formed in the P substrate
4 is disposed between two adjacent N source regions.

1 13. The semiconductor device of claim 8, wherein the epitaxial layer is
2 an N epitaxial layer.

1 14. The semiconductor device of claim 7, wherein the silicon substrate
2 is an N substrate.

1 15. The semiconductor device of claim 6 wherein the dielectric layer in
2 the second device comprises a field oxide layer.

1 16. A method of forming a trenched DMOS device, the method
2 comprising:

3 providing an N+ silicon substrate with an N epitaxial layer thereon,
4 and a P substrate in the N epitaxial layer extending to a top surface thereof;

5 forming in a device region a plurality of DMOS trenches extending
6 downward through the P substrate from a top surface thereof, and in a bus region a field
7 oxide layer on the P substrate and a bus trench extending down from a top surface of the
8 field oxide layer to a lower portion of the P substrate;

9 forming a gate oxide layer in the DMOS trenches which extends to
10 cover the top surface of the P substrate adjacent the DMOS trenches, and a gate oxide
11 layer in the bus trench which extends to cover the top surface of the P substrate adjacent
12 the bus trench;

forming a plurality of polysilicon gates in the DMOS trenches, and
a polysilicon bus in the bus trench, the polysilicon bus having a top surface disposed at a
lower level than the top surface of the field oxide layer;
forming a plurality of N⁺ source regions in the P substrate adjacent
the DMOS trenches;
forming a plurality of P⁺ diffused regions in the P substrate, each of
the P⁺ diffused regions being interposed between two of the N⁺ source regions;
forming a first isolation layer over the P substrate to cover the
polysilicon gates, and a second isolation layer to cover the field oxide layer, the second
isolation layer having an opening to expose the polysilicon bus; and
forming a source metal contact layer on the first isolation layer, and
a metal line atop the polysilicon bus, the source metal contact layer connecting to the N⁺
source regions and the P⁺ diffused regions.

17. The method of claim 16, wherein the P substrate of the device
region and the P substrate of the bus region are formed by ion implantation
simultaneously.

18. The method of claim 16, wherein the gate oxide layer of the device
region and the gate oxide layer of the bus region are formed simultaneously.

19. The method of claim 16, wherein the polysilicon gate and the
polysilicon bus are formed by depositing a polysilicon layer in the DMOS trenches and the
bus trench and using the gate oxide layers as etch stop layers to etch the polysilicon layer.

20. The method of claim 16, wherein the plurality of N⁺ source regions
are formed in the P substrate on opposite sides of each of the DMOS trenches.